GLQX0ACXX-4

QSFP+ 40G to 4*10G SFP+ 850nm XXm Active Optical Cable

Features

- QSFP to 4 SFP AOC supports high density 10GBE per channel application.
- Cable length up to 70 meters.
- Power consumption per end: <1.0W for QSFP and <0.35W for SFP+.
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage for QSFP and SFP+ • RoHS 6 compliant

Applications

- 40GbE and 10GbE break-out applications for Data-com switch and router connections
- 40G to 4×10G density applications for Data-com and Proprietary protocol applications
- Data center

General Description

The Gearlink's Technologies GLQX0ACXX-4 is a Four-Channel, Pluggable, Parallel, FiberOptic QSFP+ Active Optical Cable (AOC) to 4× SFP+ Active Optical Cable break-out solution. This Breakout cable is intended for 40G to 4× 10G applications.

This AOC is a high performance cable for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 40Gbps aggregate bandwidth. Each lane can operate at 10.3125Gbps. These cables also support 4 x 10G InfiniBand QDR applications and are backwards compatible to the 4 × 5G IB DDR and 4 × 2.5G IB single IB SDR application.

This product is leveraged from GearLink 's Technologies QSFP+ to QSFP+ Active Optical Cable product and SFP+ Active Optical Cable product. Where applicable, consult these respective data sheets.

This AOC incorporates GearLink's Technologies' proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Ordering Information

Part Number	Description
GLQX0ACXX-4	40Gb/s QSFP+ to 4x10G SFP+ Active Optical Cable

Notes:

where "xx" denotes cable length in meters. Examples are as follows:

xx = 03 for 3m, xx = 10 for 10m, xx = 50 for 50m, xx = A0 for 100m

Feature	Standard	Performance
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022:2010, Class B	Compatible with standards
Electromagnetic susceptibility (EMS)	EN 55024:2010	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product

Absolute Maximum Ratings

The operation in excess of any absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TST	-40	85	degC	
Relative Humidity(non-condensing)	RH	0	85	%	
Operating Case Temperature	TOPC	0	70	degC	
Supply Voltage	VCC	-0.3	3.6	V	
Input Voltage	Vin	-0.3	Vcc+0.3	V	

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TOPC	0		70	degC	Operating Case Temperature
Power Supply Voltage	VCC	3.13	3.3	3.47	V	Power Supply Voltage
Data Rate	DR		10.3	11.3	Gbps	Data Rate
Data Speed Tolerance	ΔDR	-100		+100	ppm	
Link Distance with OM3 fiber	D	0		100	m	
Control* Input Voltage High	Vih	2		VCC+0.3	V	
Control* Input Voltage Low	Vil	-0.3		0.8	V	
I2C Serial Interface frequency	fs			400k	Hz	
Power Supply Noise				50	mVpp	
Receiver Differential Data Output Load				100	mVpp	

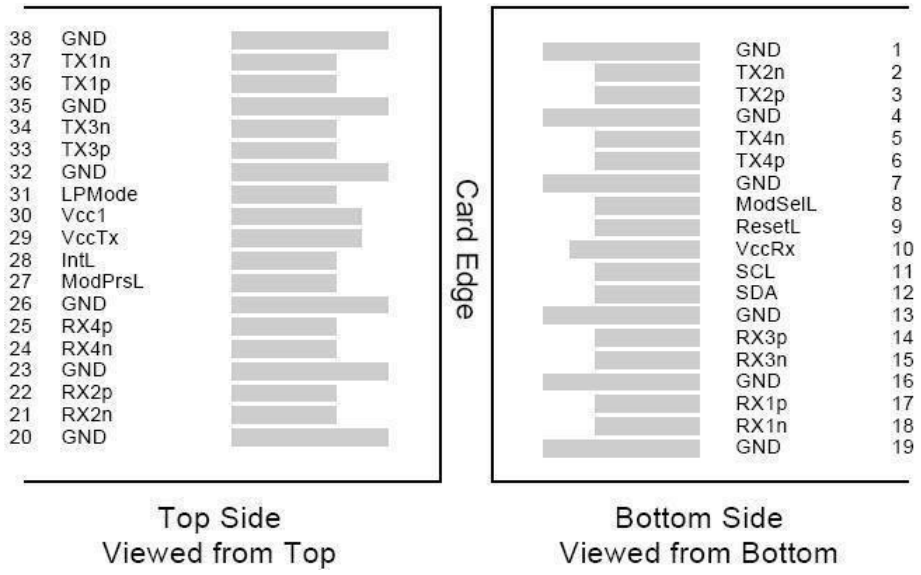
Active Cable-End Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
QSFP+ 40G Active Cable-End Power Consumption				1.0	W	
QSFP+ 40G Active Cable-End Power Supply Current				300	mA	
SFP+ 10G Active Cable-End Power Consumption				0.35	W	
SFP+ 10G Active Cable-End Power Supply Current				100	mA	

QSFP+ AOC-end Electrical Characteristics Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
Differential input voltage amplitude	ΔVin	300		1100	mVp-p	
Differential output voltage amplitude	ΔVout	400		800	mVp-p	
Bit Error Rate	BR			E-12		
Input Logic Level High	VIH	2.0		VCC	V	
Input Logic Level Low	VIL	0		0.8	V	
Output Logic Level High	VOH	VCC-0.5		VCC	V	
Output Logic Level Low	VOL	0		0.4	V	

QSFP+ AOC-end Pin Assignment and Description



QSFP+ AOC-end Pin Assignment

PIN #	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	
5	CML-I	Tx4n	Transmitter Inverted Data Input	

6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	
30		Vcc1	+3.3 V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the

ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length
(t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

GearLink’s QSFP+ SR4 operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

QSFP+ AOC-end Power Supply Filtering

The host board should use the power supply filtering shown in Figure1.

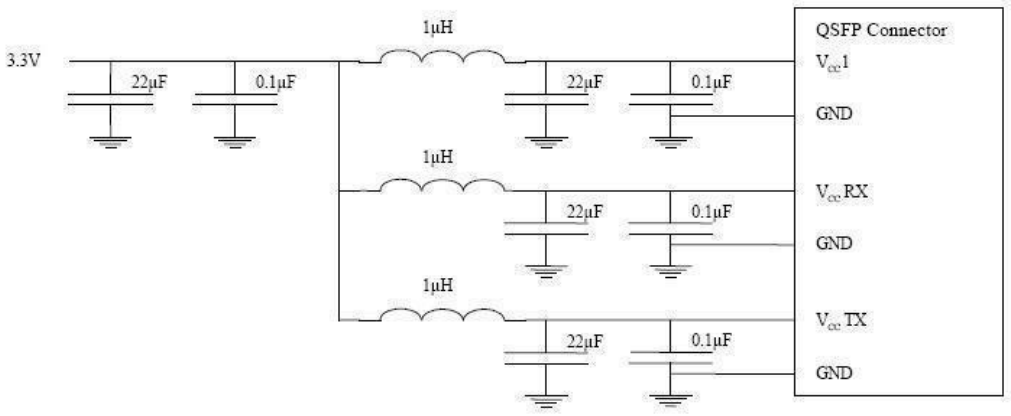


Figure1. Host Board Power Supply Filtering

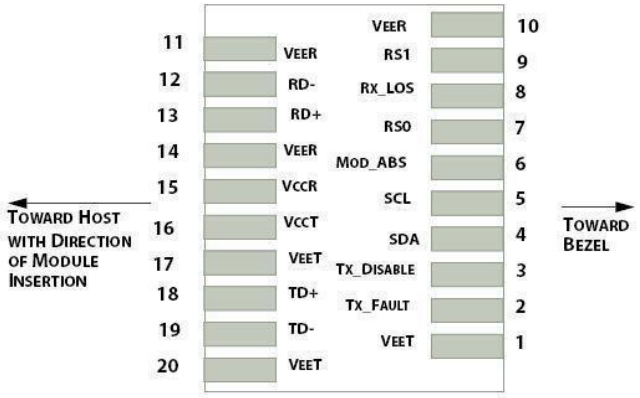
QSFP+ AOC-end EEPROM Serial ID Memory Contents:

Compliant to the industry standard SFF-8436 QSFP Specification

SFP+ AOC-end Electrical Characteristics Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	
Differential Output impedance	Zout	90	100	110	ohm	
Differential input voltage amplitude	ΔVin	100		1800	mVp-p	
Differential output voltage amplitude	ΔVout	1000		800	mVp-p	
Bit Error Rate	BR			E-12		
Input Logic Level High	VIH	2.0		VCC	V	
Input Logic Level Low	VIL	0		0.8	V	

SFP+ END Pin Assignment and Description



Pin Assignment

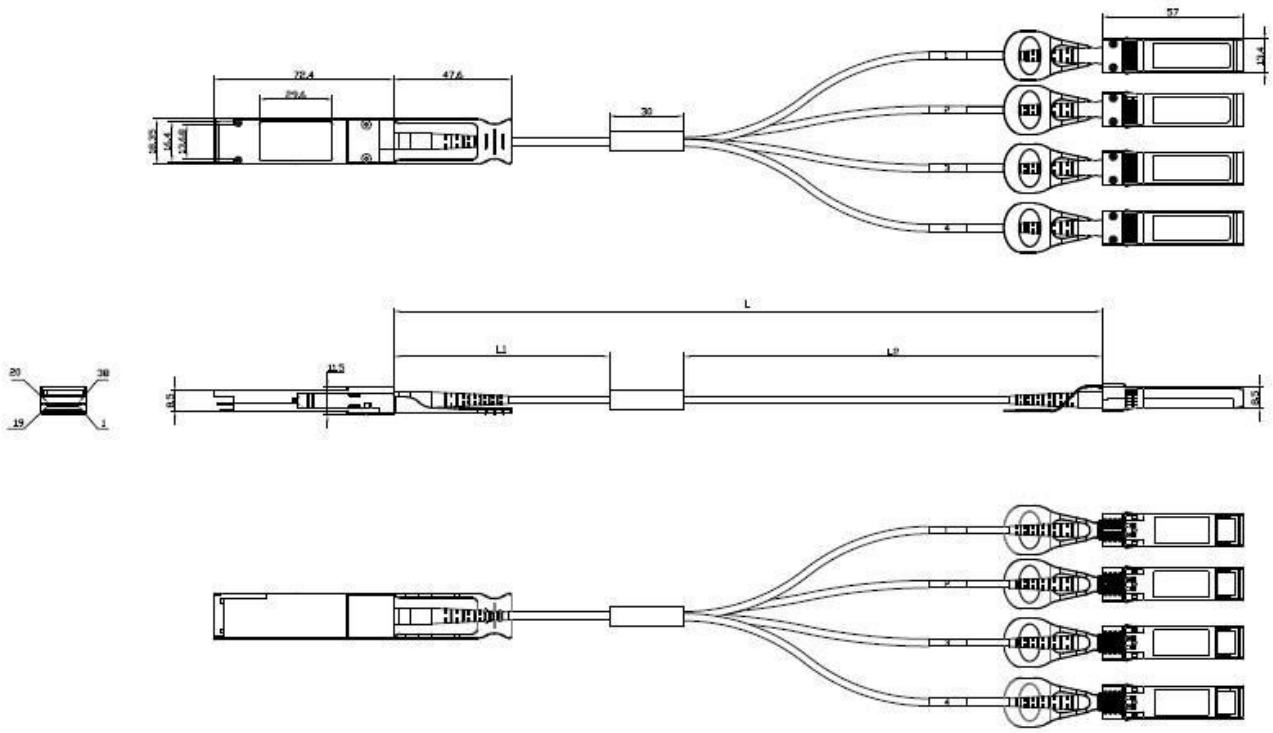
PIN #	Symbol	Description		Notes
1	VeeT	Transmitter Signal Ground	Note 1	
2	TX_FAULT	Transmitter Fault (LVTTL-O) – Not used. Grounded inside the module	Note 2	
3	TX_DISABLE	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	Note 3	
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O) (same as MOD-DEF2 in INF-8074)	Note 4	
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O) (same as MOD-DEF1 in INF-8074)	Note 4	
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	Note 5	
7	RS0	Rate Select 0 - Not used, Presents high input impedance.		
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	Note 2	

9	RS1	Rate Select 1 - Not used, Presents high input impedance.		
10	VeeR	Receiver Signal Ground	Note 1	
11	VeeR	Receiver Signal Ground	Note 1	
12	RD-	Receiver Data Out Inverted (CML-O)		
13	RD+	Receiver Data Out (CML-O)		
14	VeeR	Receiver Signal Ground		
15	VccR	Receiver Power + 3.3 V		
16	VccT	Transmitter Power + 3.3 V		
17	VeeT	Transmitter Signal Ground	Note 1	
18	TD+	Transmitter Data In (CML-I)		
19	TD-	Transmitter Data In Inverted (CML-I)		
20	VeeT	Transmitter Signal Ground	Note 1	

Notes:

1. **Module circuit ground is isolated from module chassis ground within the module. GND is the symbol for signal and supply (power) common for SFP modules.**
2. **This is an open collector/drain output that on the host board requires a 4.7kΩ to 10kΩ pullup resistor to VccHost. See Figure 2.**
3. **This input is internally biased high with a 4.7kΩ to 10kΩ pullup resistor to VccT.**
4. **Two-Wire Serial interface clock and data lines require an external pullup resistor dependent on the capacitance load.**
5. **This is a ground return that on the host board requires a 4.7kΩ to 10kΩ pullup resistor to VccHost.**

Mechanical Dimensions



ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Ordering Information

Part Number	Description
GLQX0ACXX-4	40Gb/s QSFP to 4x10G SFP+ Active Optical Cable

Notes:

where "xx" denotes cable length in meters. Examples are as follows:

xx = 03 for 3m, xx = 10 for 10m, xx = 50 for 50m, xx = A0 for 100m