GDQ1M0C85

400Gb/s QSFP-DD SR8 Optical Transceiver Moudule

General Description

Centera's 400-Gbps QSFP-DD SR8 Optical Transceiver Module (400G QSFP-DD SR8) with Quad Small Form-Factor Pluggable Double Density (QSFP-DD) form-factor is of high performance in bi-directional signal transmission and aggregate 400Gbps bandwidth, which design to follow QSFP DD MSA and 200GBASE-SR4 of IEEE 802.3cd standard.

Compared with the conventional copper-based direct attach cables (DACs), the optical fiber with pluggable MPO connector enables the ease of complicated data center cabling deployment by the longer, lighter, and bendable characteristics. The optical transceiver module utilizes high-performance 850-nm GaAs VCSELs and PIN PDs with superior integration in signal integrity and optical sub-assembly, whose bit-error-rate is better than 2.4 E-4 for reliable packet communication within data center.

Features

- Compliance to 200GBASE-SR4 of IEEE 802.3 cd Rev. 3.2
- Compliance to QSFP DD MSA Rev 3.0 (for Memory Map) and 4.0 (for Mechanical QSFP-DD Housing)
- Supports 400 Gbps data rate links up to 70m/100 m via OM3/OM4, respectively.
- Typical Power Consumption: 10W (each port)
- Hot pluggable electrical interface
- Adopt either standard 2 Row by 12-channel or 1 Row by 16-channel MPO connectors inside module
- 0 to 70° C case temperature operating range
- RoHS-6 Compliant (lead-free)

Application

- Ethernet for 200GBASE-SR4
- For 400 Gb/s Ethernet Application
- HPC Interconnects
- Proprietary Interconnections

Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	oC	
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5		Vcc+0.5	
Control Input Voltage	-0.5	3.6	V	1
Relative Humidity	5	85	%	
Rx Optical Damage Threshold / Lane	5		dBm	

Notes: 1. Non-condensing.

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	°C	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel			26.5625	Gbps	
Bit Error Ratio (BER)			$2.4x10^{-4}$		1, 2
Control Input Voltage High	2		Vcc+0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock			1	MHz	
Differential Data Input / Output Load		100		Ohms	+/- 10%
Fiber Length: 2000 MHz·km 50/125μ m MMF			70	m	
Fiber Length: 4700 MHz·km 50/125μ m MMF			100	m	

Notes:

1. Bit-Error-Rate (BER) is tested with PRBS 31Q pattern.

2. 400G QSFP-DD SR8 requires an electrical connector compliant with QSFP-DD MSA which is used on the host board in order to guarantee its electrical interface specification.

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics						
TRx Power Consumption			10	12	W	
TRx Power-on Initialization Time				2000	ms	
400GAUI-8 Module Electrical Input Characteristics (TP1)						
Single Ended Input Voltage Tolerance		-0.4		3.3	V	
Differential pk-pk input voltage				880	mV	
Differential Input Return Loss	Sdd11				dB	1
Common to differential mode	Scd11				dB	2
DC common mode voltage		-0.3		2.8	V	
400GAUI-8 Module Electrical Output Characteristics (TP4)						
AC Common-Mode Output Voltage				17.5	mV	
Differential Output Voltage				900	mV	

Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Near-end Eye Height		70			mV	
Far-end Eye Height		30			mV	
Differential Output Return Loss	Sdd22				dB	1
Common to Differential Mode	Scd22				dB	2
Transition Time (20% to 80%)		9.5			ps	
DC Common Voltage		-350		2850	mV	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Center Wavelength	λ	840		860	nm	
Spectral Width – RMS	Δλ			0.6	nm	
Average Launch Optical Power, each lane	LOP	-6		4	dBm	
Optical Modulation Amplitude, each lane	OMA	-4		3	dBm	
Launch power in OMA minus TDEC		-5.9			dBm	
Transmitter and dispersion eye closure	TDECQ			4.9	dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction ratio	ER	3			dB	
Optical return loss tolerance				12	dB	
Encircled Flux		≥ 86% @ 19um,				
Receiver Optical Characteristics						
Center wavelength, each lane	λ	840		860	nm	
Damage Threshold		5			dBm	
Average power at receiver input, each lane		-7.9		4	dBm	1
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity (OMAouter)		See Eq. 3			dBm	2,3
Stressed receiver sensitivity in OMA				-3	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure (SECQ), lane under test			4.9		dB	
OMA of each aggressor lane			3		dBm	

Notes:

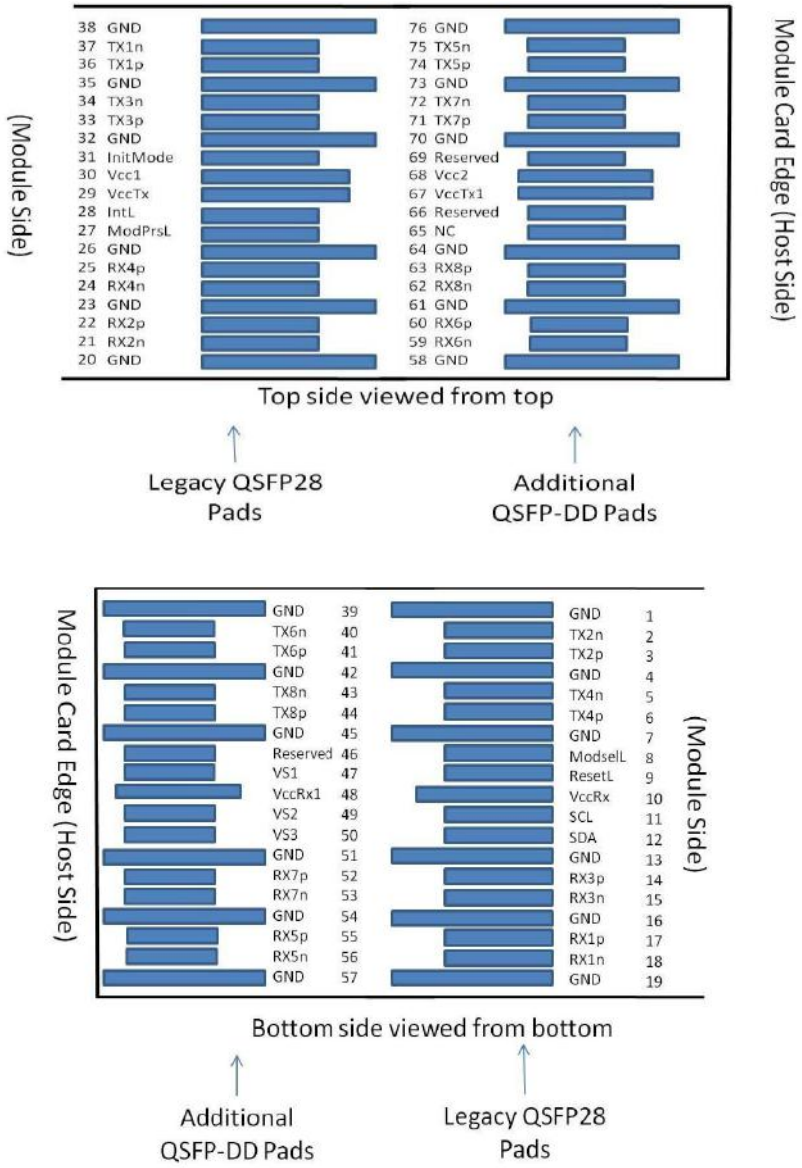
1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.9 dB.

3. Equation 3: RS= Max (-6, SECQ-7.9) (dBm), where RS is the receiver sensitivity SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

4. Measured with conformance test signal at TP3 for the BER of 2.4 E-4

QSFP-DD Module Pad Assignments and Descriptions



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	1
16		GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note

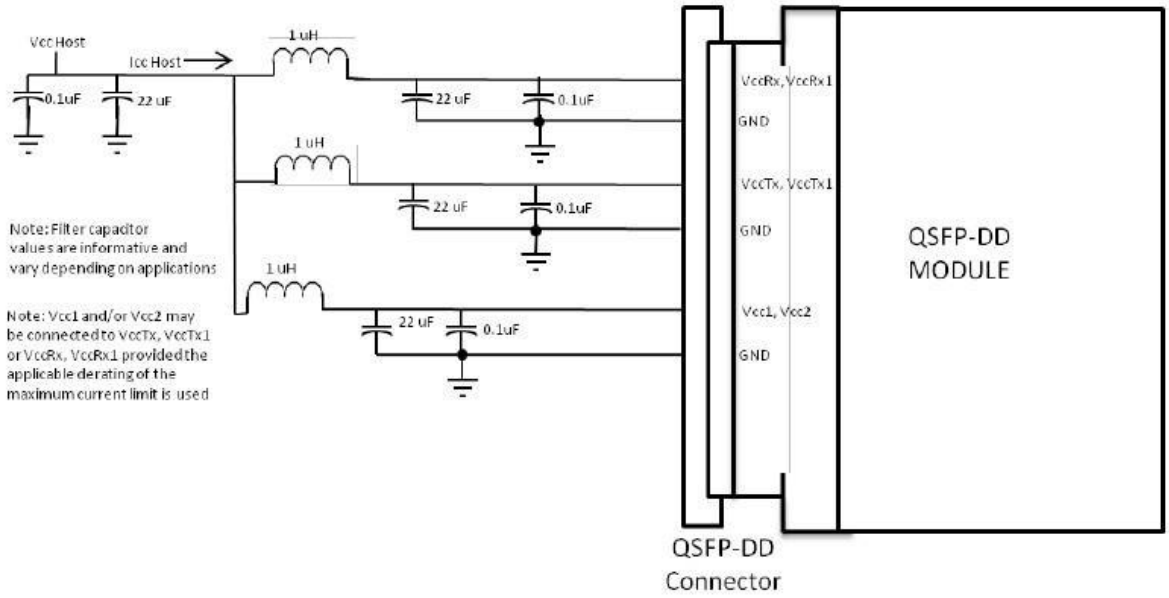
1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

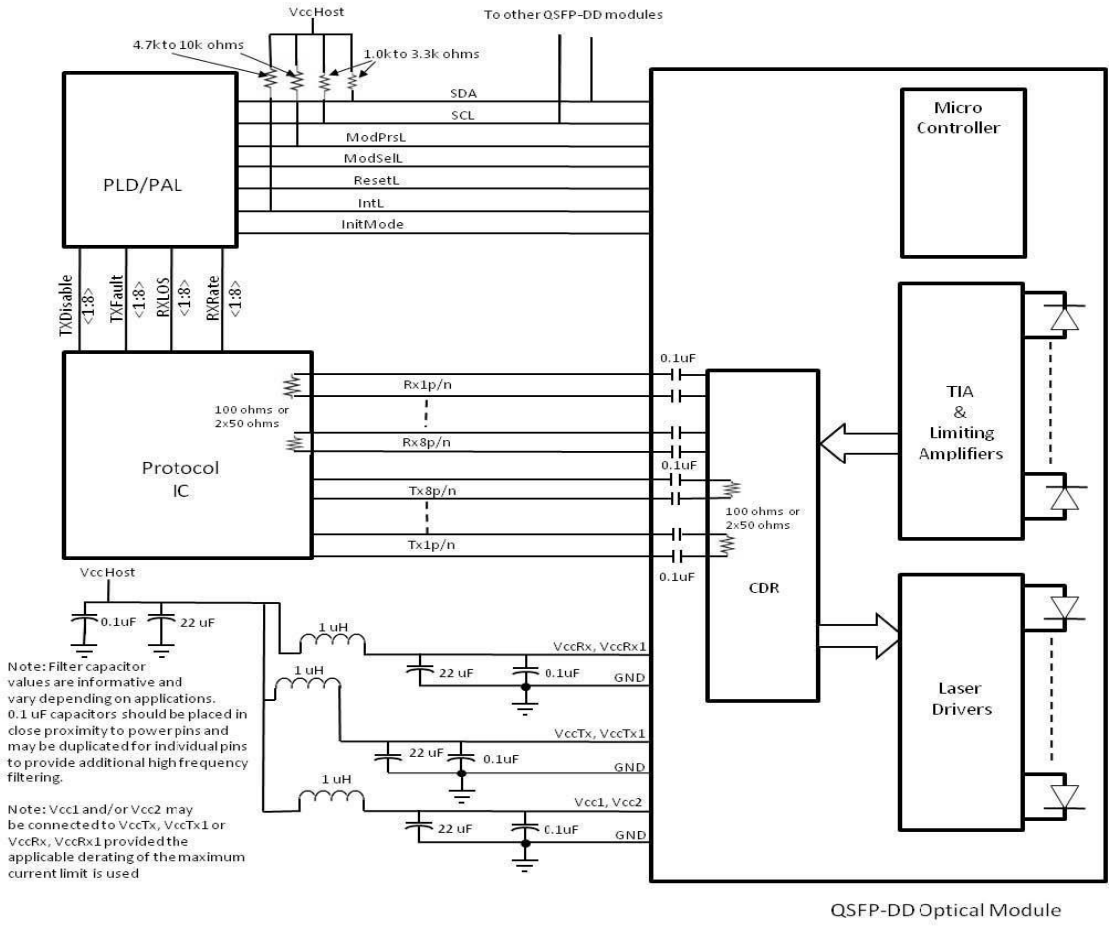
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

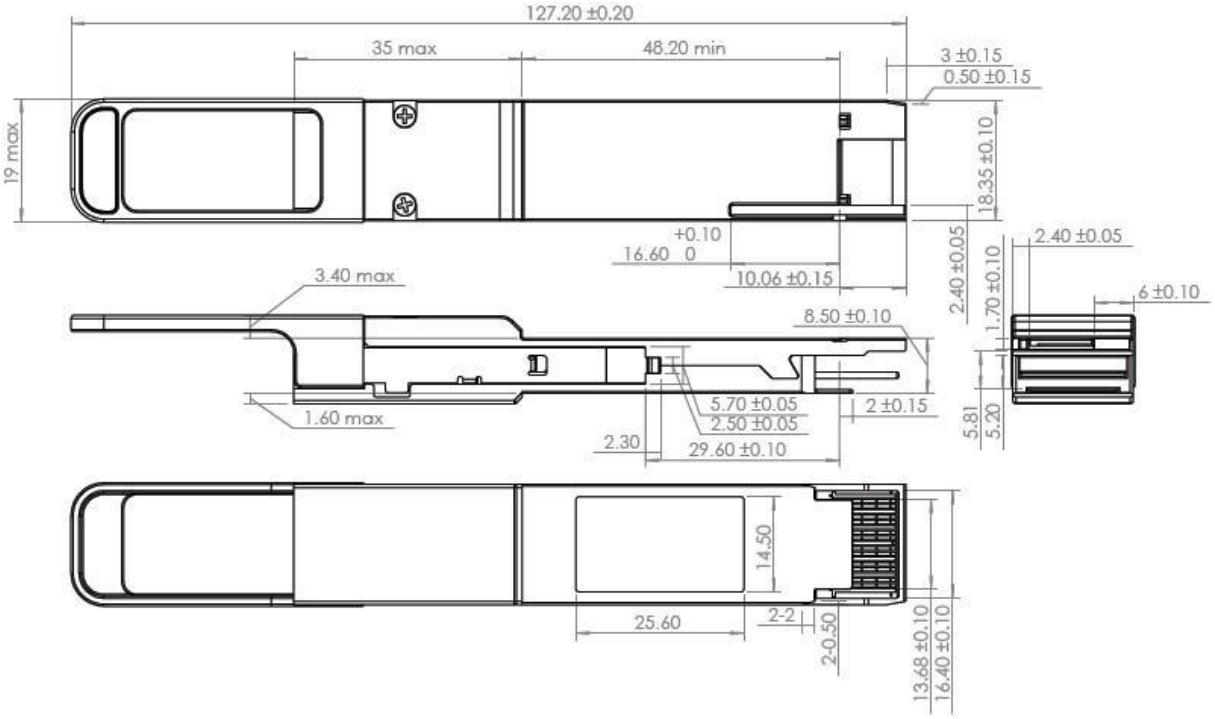
Recommended Host Board Power Supply Circuit



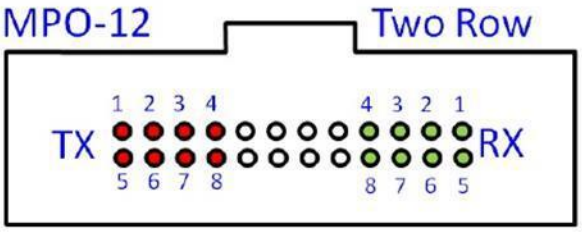
Recommended Interface Circuit



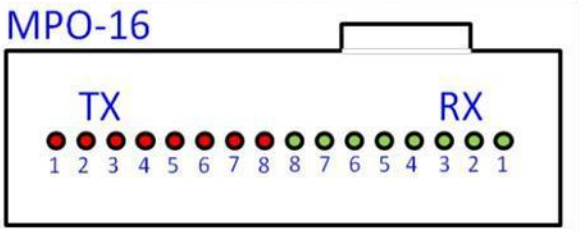
Mechanical Design Diagram



Optical-Channel Definition for
2 Row x 12C Fiber

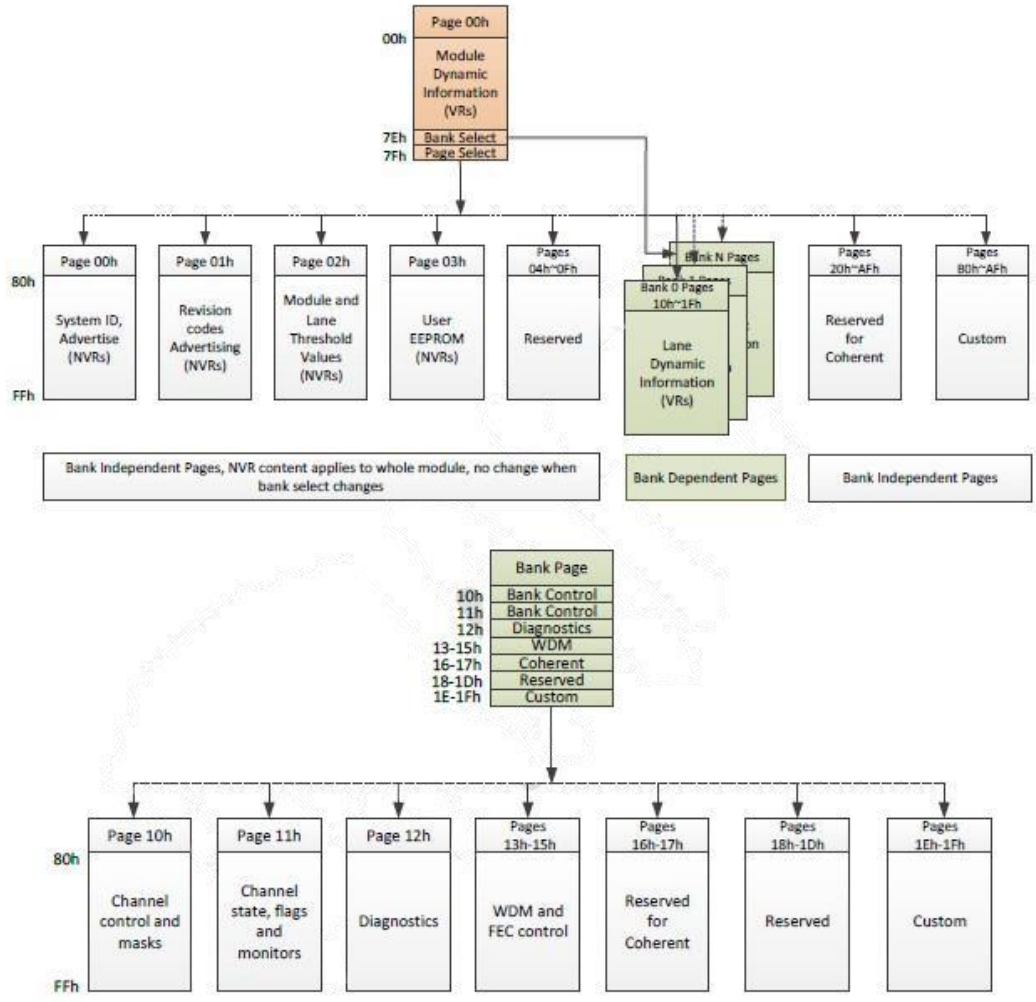


Optical-Channel Definition for
1 Row x 16C Fiber



Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP-DD rev.3.0 specification as shown in the below. For more detailed description of this memory map, please see our Memory Map document with flexible customization settings.



Regulatory Compliance Table

Item	Compliance	Note
Electrostatic Discharge (ESD) to the	JEDEC Human Body Model (HBM)(JESD22-A114-B)	
Electrostatic Discharge (ESD)	EN 61000-4-2	
Electromagnetic Interference (EMI)	47 CFR FCC Rules and Regulations Part 15 Subpart B, Class B Digital Device	
	EN 55032:2015/AC:2016, Class B	
Immunity	EN 55024:2010/A1:2015	
Laser Safety	EN 60825-1:2007 and IEC 60825-1:2014	CLASS 1 LASER