GJS3L0C31

SFP28 25G 1310nm 10km DDM GJS3L0C31

Features

- Up to 24.33Gb/s for CPRI
- Up to 25.78Gb/s for bi-directional data links
- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8432 and SFF-8472
- Build-in dual CDR with shut off control
- SFP28 MSA package with duplex LC connector
- Uncooled 1310nm DFB Laser
- Up to 10 km on 9/125um SMF
- Single +3.3V power supply
- Class 1 laser safety certified
- 1.0W maximum power consumption with established link
- Operating temperature Options:
  YV0D-C03: 0℃ to 70℃;
  YV0D-I03: -40℃ to 85℃
- RoHS Compliant

Applications

- High speed storage area networks
- 25G high speed interconnection
- 24.33G CPRI

Description

GJS3L0C31 SFP28 transceivers, according to 25 Gigabit Small Form Factor Pluggable “SFP28” Multi-Sourcing Agreement (MSA) SFF-8431 Rev.
4.1 and SFF-8472 Rev. 12.1, are designed for use up to 25.78Gb/s data rate and up to 10km link length. They are compatible with SFF-8432.

Specification

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	℃
Supply Voltage	V_{CC3}	-0.5	4.0	V
Relative Humidity(Non-condensing)	RH	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0	25	70	℃
	T_C	-40	25	85	℃
Power Supply Voltage	V_{CC3}	3.135	3.3	3.465	V
Data Rate	-	-	24.33 25.78	28	Gbps

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Module Supply Current	Icc	-	-	300	mA	-
Power Dissipation	PD	-	-	1000	mW	-
Transmitter			-	-		-
Input Differential Impedance	ZIN	-	100		Ω	
Differential Data Input Swing	VIN, P-P	180	-	700	mVP-P	
TX_FAULT Transmitter Fault Normal Operation	VOH	2.0	-	VCCHOST	V	
	VOL	0		0.8	V	
TX_DISABLE Transmitter DisableTransmitter Enable	VIH	2.0	-	VCCHOST	V	
	VIL	0		0.8	V	
Receiver						
Output Differential Impedance	ZO		100		Ω	
Differential Data Output Swing	VOUT, P-P	300	-	850	mVP-P	1
Data Output Rise Time, Fall Time	tr, tf	15	-	-	ps	2
RX_LOS Loss of signal (LOS)Normal Operation	VOH	2.0	-	VCCHOST	V	3
	VOL	0	-	0.8	V	3

Transmitter Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Launch Optical Power	Po	-7	-	2	dBm	1
Extinction Ratio	ER	3	-	-	dB	
Center Wavelength Range	λc	1295	1310	1325	nm	
Optical Modulation Amplitude	OMA	-4	-	2.2	dBm	
Transmitter and Dispersion Penalty	TDP	-	-	2.7	dB	
Spectral Width	Δλ	-	-	1	nm	
$RIN_{20}OMA$	-	-	-	-130	dB/Hz	
Optical Return Loss Tolerance	ORLT	-	-	20	dB	
Pout @TX-Disable Asserted	Poff	-	-	-20	dBm	
Eye Diagram	25GBASE-LR mask and filter					

Notes:

1. Average optical power shall be measured using the methods specified in TIA/EIA-455-95.

Receiver Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Center Wavelength	λc	1295	1310	1325	nm	-
Receiver OMA Sensitivity	RxSENS	-	-	-12	dBm	1
Receiver Overload (OMA)	Pol	2.2	-	-	dBm	1
Receiver Reflectance		-	-	-26	dB	-
LOS De-Assert	LOSD	-	-	-13	dBm	-
LOS Assert	LOSA	-30	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

Notes:

1.Receiver sensitivity is informative. shall be measured with conformance test signal for BER =5x 10-5 .

Special function

Receiver special description are defined in table as below.

Parameters	Description	Note
RX LOS RX LOS enable/disable	RX LOS enable	*1
LOS LOS Criterion	OMA	

Note:

RX LOS enable means when LOS RX no signal output, inverse, Rx may be have normal signal amplitude output.

Pin-out Definition

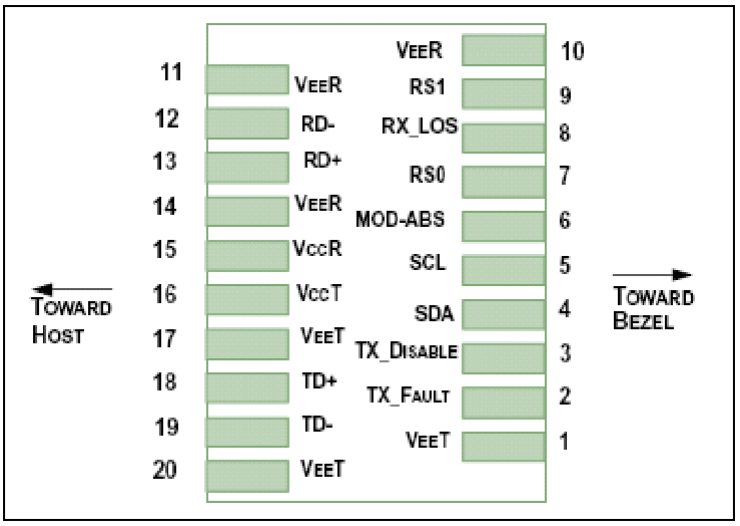


Figure1

Pin Description

Pin	Symbol	Name/Description	Note
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	NA	6
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	2
9	RS1	NA	6
10	VccRx	Receiver Ground	1
11	SCL	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	
13	RD+	Received Data out (CML-O)	
14	VeeR	Receiver Ground	
15	VccR	Receiver Power - +3.3V	
16	VccT	Transmitter Power - +3.3 V	
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	
19	TD-	Inverse Transmitter Data In (CML-I)	
20	VeeT	Transmitter Ground	1

Notes:

1.The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.

2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10kohms to Host_Vcc on the host board. Pull ups can be **connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.**

3.This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10kohms to VccT in the module.

4. See sff-8431 4.2 2-wire Electrical Specifications .

5.This pin shall be pulled up with 4.7k-10kohms to Host_Vcc on the host board. [6]If implementing SFF-8079 pin 7 and 9 are used for AS0 and AS1 respectively.

Board Power Supply Filter Network

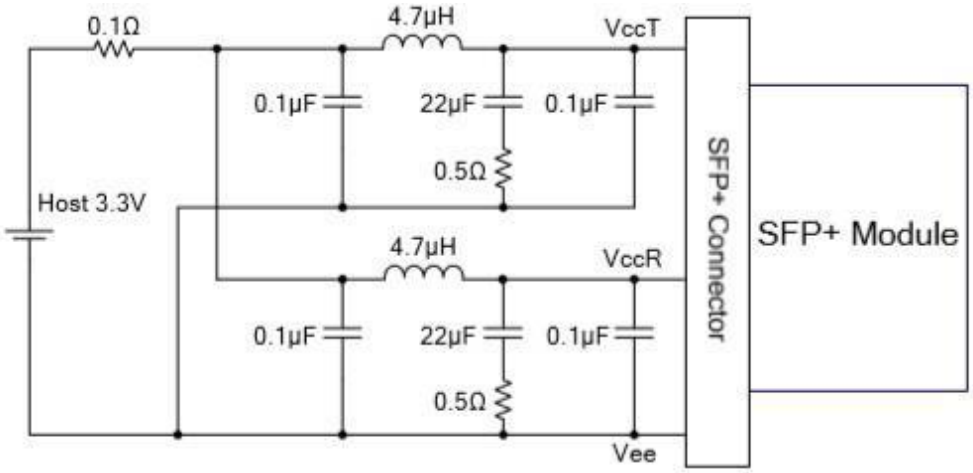


Figure2

Recommended Interface Circuit

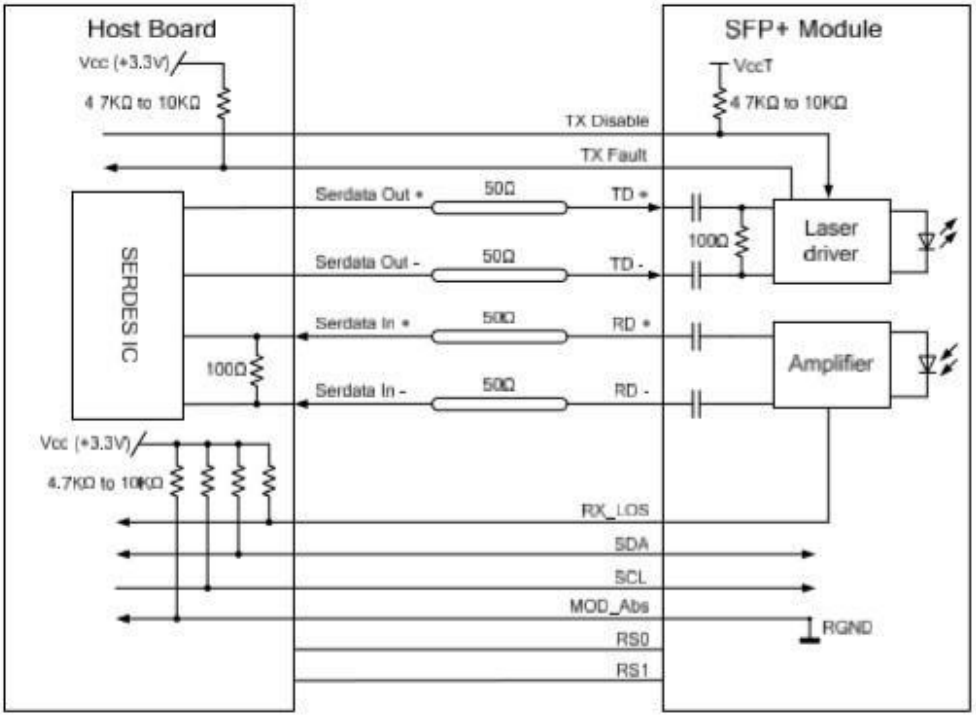


Figure3

Dimensions

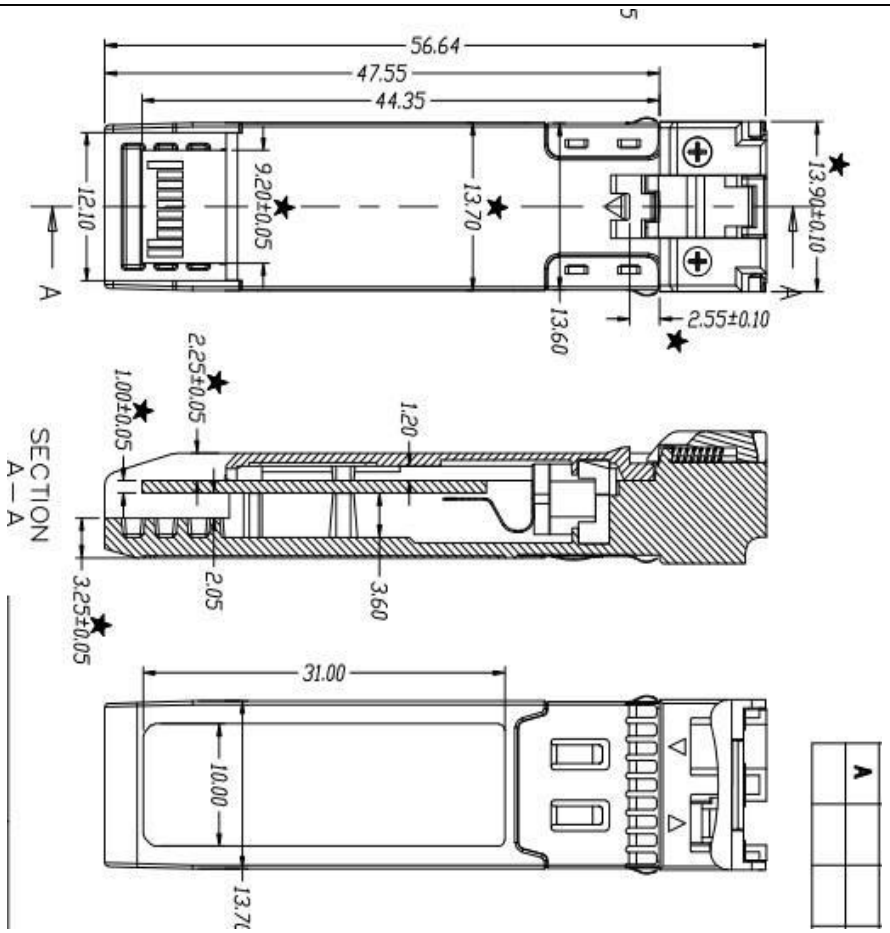
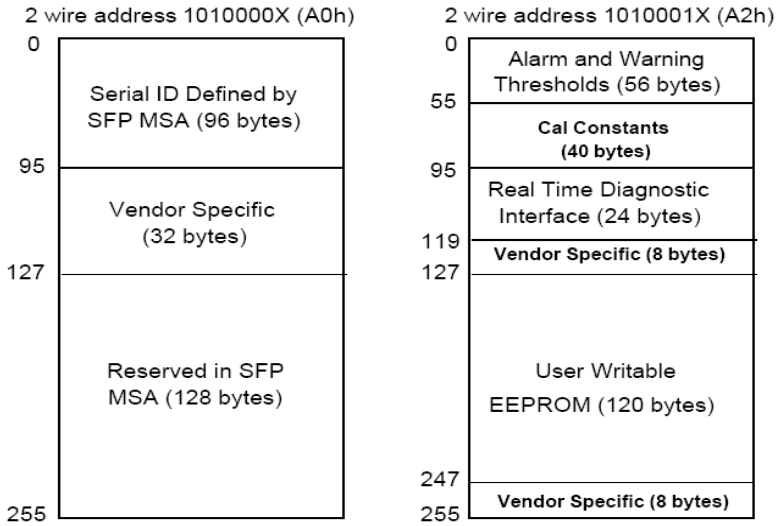


Figure4

Digital Diagnostic Memory Map



Ordering Information

Part No	Tx	Pout	Rx	S	Top	Reach	RoHS	DDM
GHS3L0C31	1310nm DFB	-7～2dBm	PIN	<-12dBm	0~70℃	10km	Compliant	Available